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EXAMINER	
ENGLUND, TERRY LEE	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 07/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SN

Office Action Summary	Application No.	Applicant(s)	
	10/603,217	EDWARDS, ERIC E.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *May 10, 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-4,6,7,9-13,19,20,22 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13 and 19* is/are allowed.

6)☒ Claim(s) *2-4,6,7,9-12,22 and 23* is/are rejected.

7)☒ Claim(s) *20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The amendment submitted on May 10, 2005 was reviewed and considered with the following results:

The cancellation of claims 5 and 21 render their respective objection and/or rejection moot.

The amended claims overcame the objections to claims 2-3, and 6 as described in the previous Office Action. Therefore, those objections have been withdrawn. However, after reconsidering the claims, oversights with respect to claims 10 and 20 were noted. These are described later under the appropriate section.

The amended claims also overcame the rejections of claims 2-4, and 6-7 under 35 U.S.C. 112, which have now been withdrawn. However, newly added claims 22-23 have their own respective rejection(s), which are described later under the appropriate section.

The previous Office Action's rejection of claim 7, with respect to "the hysteresis" problem has been withdrawn. That rejection had been made due to insufficient antecedent basis within the Nov 8, 2004 amendment's version of claim 7. Although identifying the claim as being "(Original)", that amendment's claim 7 depended on claim 4, which does not cite "a hysteresis circuit." However, the present amendment's version of claim 7, also identified as being "(Original)", accurately corresponds to the original claim 7, wherein claim 7 actually depends on claim 6, which provides the proper antecedent basis for "the hysteresis circuit."

The prior art rejections of claims 2-4 under 35 U.S.C. 102(b), with respect to Tabata, and of claims 6-7 under 35 U.S.C. (a), with respect to Tabata/Degoirat et al., have now been

withdrawn. The Tabata reference does not show or disclose "a plurality of second diode connected transistors" as now recited within amended independent claim 4, upon which claims 2-3 and 6-7 depend.

Some of the previous Office Action's other prior art rejections have also been withdrawn. These include: 1) claims 2-4 under 35 U.S.C. 103(a) with respect to Frisch et al.; and 2) claims 2-4 under 35 U.S.C. 103(a) with respect to Guritz.

However, the rejections of claims 9-12 under 35 U.S.C. 103(a) with respect to Guritz/Furuchi; and of claims 9-12 under 35 U.S.C. 103(a) with respect to Frisch et al./Furuchi have been basically maintained, with some modifications to further clarify the examiner's position.

Therefore, modified rejections of claims 2-4, 6-7, and 9-12 are described later. These rejections further clarify the examiner's reasoning, and/or provide an example of one reference that uses a plurality of diode connected transistors. Related comments are described under the Response to Arguments section.

Claim Objections

Claims 10 and 20 are objected to because of the following informalities: To minimize possible confusion with respect to the "reset signal" and the "output node" recited within independent claim 12 (e.g. see lines 10-11), and the output states recited within dependent claim 10, the following changes to claim 10 are suggested: 1) add --the reset signal as-- after "provides" on line 2; 2) add --node-- after the second occurrence of "output" on line 2; and 3) change "state or a" to --state and a-- on line 3. The first two changes will clearly relate the "output signal" and "the output" of claim 10 back to the "reset signal" and "an output node" of

claim 12. The third change more clearly indicates the two distinct states of the "two state output signal" as being the first/high output state, and the second/low output state. Dependent claim 20 has the same type of problems with independent claim 13 that claim 10 has with claim 12. Therefore, it is suggested claim 20 be changed in the same manner as described above with claim 10. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 22-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. Claim 22 recites "a third resistor" on line 5, implying a second resistor that has not been identified within the claim's chain of dependency. It is not clear if the feedback transistor is actually connected "in parallel" with the diode connected transistor(s) as recited within each of claims 22 and 23, or if --in series-- was meant. For example, in the applicant's own Figs. 9 and 10, feedback transistor T7 is coupled in parallel with resistor R2, but it is coupled in series with diode connected transistor T6. Also, since the third resistor is connected in parallel with the feedback transistor, and the feedback transistor is connected in parallel to the diode connected transistor(s), then the third resistor is also connected in parallel to the diode connected transistor(s). Therefore, how would this structure actually function, and where is this shown and disclosed?

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-4 are now rejected under 35 U.S.C. 103(a) as being unpatentable over Frisch et al. (Frisch), in view of Payne et al. (Payne), wherein both of these references were cited on previous PTO-892s with respect to this application. Fig. 4 of Frisch shows power up reset circuit 20 comprising comparator 38 (or 38,40) with first/second inputs 29/36 and output 41 (or 46); first diode is connected transistor 24 connected between first input 29 and power supply voltage Vdd; first resistor 26 is connected between first input 29 and ground potential Vss; second diode is connected transistor 34 coupled between second input 36 and ground potential Vss, wherein a reset signal at output 41 (or 46), corresponding to signal POR, is generated when the voltages at first/second inputs 29/36 are approximately the same (e.g. see the lower right graph showing Vdd, 29, 36, and 46). Although Frisch does not show a plurality of first diode connected transistors 24, and a plurality of second diode connected transistors 34, Frisch does disclose "Modifications can readily be made by those skilled in the art consistent with the principles of this invention." on column 9, lines 3-7. One of ordinary skill in the art would understand the invention's principles relate to using a comparator to provide a power-on reset signal when two compared voltages, each having a different varying rate, cross at a predetermined point during the power-up sequence. When, and where, they cross will be determined by the structures within input circuits 22 and 30. Payne shows a power-on reset circuit in Fig. 3 with a plurality of diode

connected transistors 305, and more importantly, teaches "it is obvious to a person of ordinary skill in the art that many diodes can be stacked in series to set a higher threshold voltage" (e.g. see column 4, lines 64-66). Therefore, one of ordinary skill in the art would understand that it would have been obvious to replace Frisch's single diode connected transistor 24, and single diode connected transistor 34, with a respective plurality (e.g. at least two) of series connected transistors that are each diode connected, thus rendering claim 4 obvious. The plurality of first and second transistors would provide a means for delaying when the reset signal is actually generated, which corresponds to when power supply voltage Vdd reaches a higher voltage level. For example, the voltage at first input 29 would not begin to increase from ground until the power supply voltage has reached at least the combine threshold voltage of all of the series connected transistors 24. [Using the upper graph of Fig. 4 as a reference, when transistor 24 is replaced by at least two diode connected transistors, which are coupled in series, line 29 would shift farther to the right.] With respect to the plurality of second diode connected transistors, the voltage at second input 36 would not begin to stabilize (e.g. level off) until power supply voltage Vdd has reached at least the combined threshold voltage of all of the series connected transistors 34. [Using the lower left graph of Fig. 4 as a reference, when transistor 34 is replaced by at least two diode connected transistors, that are coupled in series, line 36 would start to divert away from Vdd at a higher voltage, and at a later time.] The plurality of first diode connected transistors 24 would maintain at least one threshold voltage difference from power supply voltage Vdd at first input 29, rendering claim 2 obvious. The plurality of second diode connected transistors 34 would maintain at least one threshold voltage difference from ground potential Vss, and claim 3 is also rendered obvious.

Claims 2-4 are now rejected under 35 U.S.C. 103(a) as being unpatentable over Guritz, in view of Payne et al. (Payne), wherein both references had been cited in at least one previous Office Action. Fig. 9 of Guritz shows power up reset circuit 10 comprising comparator 14 having first/second inputs V1/V2 and output 16 for providing the generated reset signal POWER-UP SIGNAL. The first/second inputs are coupled to circuit blocks 18/20 respectively, which can correspond to the various networks shown in Figs. 3a, 4a, 4b, 5a, and 5b (e.g. see column 4, lines 37-40), wherein the 18/20 combination provides signals V1/V2 that cross (e.g. see Figs. 6-8). Since Guritz discloses the LOAD (e.g. see Figs. 4a, 4b, 5a, and 5b) can be a resistor (e.g. see column 3, lines 35-36), the following descriptions will assume the LOAD is a resistor. Although the Guritz reference does not clearly show or disclose a plurality of diode connected transistors connected in series between an input and either a power supply voltage or ground potential, Guritz does disclose that "it is to be understood that various changes, substitutions and alterations may be made therein without departing from the spirit and scope of the invention" on lines 8-11 of column 5. One of ordinary skill in the art would understand the spirit and scope of the invention relate to using a comparator to provide a power-on reset signal when two compared voltages, each having a different varying rate, cross at a predetermined point during the power-up sequence. When, and where, they cross will be determined by the structures within sections 18 and 20 of portion 12. Since Guritz discloses different combinations of the structures could be used to obtain the suitable characteristic curves (e.g. see columns 3 (lines 7-9, 29-41, and 63-67) and 4 (lines 28-40)), one combination can have a diode connected transistor connected between the first input (e.g. V1/VR) and power supply voltage VDD (e.g. see Figs. 4a and 5a), and another diode connected transistor connected between the other input (e.g. V2/VR)

and ground (e.g. see Figs. 4b and 5b). As previously described above, with respect to the Frisch/Payne rejection, Payne shows and teaches the use of a plurality of series connected diodes (e.g. diode-connected transistors). Therefore, it would have been obvious to one of ordinary skill in the art, and supported by Payne's teachings, that each single diode connected transistor of Guritz (e.g. see T1, T3, T4, and T2 in Figs. 4a, 4b, 5a, and 5b, respectively) could be replaced by a respective plurality (e.g. at least two) of diode connected transistors coupled in series. Corresponding to the combination described above (i.e. the related structure of Fig. 4a or 5a being connected to first input V1, and the related structure of Fig. 4b or 5b being connected to second input V2), claim 4 is rendered obvious. The plurality of first and second transistors would provide a means for delaying when the reset signal is actually generated, which corresponds to when power supply voltage VDD reaches a higher voltage level, and at a later time. Using the circuit structures of Fig. 4a and Fig. 5b as an example of the selected combination, the voltage at first input V1 would not begin to increase from ground until the power supply voltage VDD has reached at least the combined threshold voltage of all of the diode connected transistors connected between first input V1/VR and power supply voltage VDD, and the voltage at second input V2 would not begin to stabilize (e.g. level off) until power supply voltage VDD has reached at least the combined threshold voltage of all of the diode connected transistors connected between second input V2/VR and ground. 34. Therefore, the plurality of first diode connected transistors would maintain at least one threshold voltage difference from power supply voltage VDD at first input V1/VR, and the plurality of second diode connected transistors would maintain at least one threshold voltage difference from ground potential VSS at second input V2/VR, rendering respective claims 2 and 3 obvious. By varying

how many diode connected transistors are coupled in series, one of ordinary skill in the art would be able to set the cross-over point (i.e. when the voltage levels on first input V1 and second input V2 meet) to a desired level the power supply voltage VDD must reach before the reset signal is generated.

Claims 6-7 are now rejected under 35 U.S.C. 103(a) as being unpatentable over Frisch/ Payne as applied to claim 4 above, in view of Degoirat et al. (Degoirat), another reference cited in the previous Office Action. As previously described, it would have been obvious to one of ordinary skill in the art to combine the references of Frisch and Payne to have a power up reset circuit comprising first/second pluralities of diode connected transistors, and a comparator. However, the references do not show or disclose a hysteresis circuit. Degoirat shows and discloses various hysteresis type circuits with respect to a voltage divider that provides a voltage to one input of a comparator of a power up reset circuit. For example, Fig. 4 shows an unlabeled switch coupled in parallel to resistor R2 of resistor divider R1-R3. This configuration allows the switching threshold of the comparator to be changed to avoid instabilities (e.g. see column 4, lines 10-26). Therefore, it would have been obvious to one of ordinary skill in the art to apply the teachings of Degoirat to modify one of the voltage divider type circuits 22 and 30 of Frisch to have a hysteresis circuit (e.g. the unlabeled switch). For example, the switch could be connected in parallel across one or more of the diode connected transistors as one means for changing the threshold voltage of when the comparator will generate the reset signal. The hysteresis circuit will help avoid instabilities with respect to the power supply voltage VDD being close to the switching threshold. For example, near the switching threshold of the comparator, noise or fluctuations on the power supply voltage or ground potential could inadvertently trigger the

comparator if no hysteresis circuit is used. Therefore, the use of Degoirat's hysteresis circuit/voltage divider teaching will effectively make the overall Frisch/Payne power up reset circuit less susceptible to noise, rendering claim 6 obvious. When the switch (across the at least one diode connected transistor) is closed (or opened, depending on where it is located), the corresponding voltage is effectively lowered, causing the switching threshold to be changed. Therefore, the hysteresis circuit effectively lowers the power supply voltage to the comparator of the power up reset circuit, and this changes the point in time when the reset signal will be generated, thus claim 7 is rendered obvious.

Claims 6-7 are now rejected under 35 U.S.C. 103(a) as being unpatentable over Guritz/Payne as applied to claim 4 above, also in view of Degoirat et al. (Degoirat). As previously described, it would have been obvious to one of ordinary skill in the art to combine the references of Guritz and Payne to have a power up reset circuit comprising first/second pluralities of diode connected transistors, and a comparator. However, the references do not show or disclose a hysteresis circuit. As previously described above, Degoirat shows and discloses various hysteresis type circuits with respect to a voltage divider that provides a voltage to one input of a comparator of a power up reset circuit. For the same type of reasoning as applied above with respect to the Frisch/Payne/Degoirat rejections of claims 6-7, it would have been obvious to one of ordinary skill in the art to modify one of the voltage divider type circuits 18 and 20 of Guritz to include a hysteresis circuit (e.g. the unlabeled switch) of Degoirat. The use of Degoirat's hysteresis circuit/voltage divider teaching will effectively make the overall power up reset circuit less susceptible to noise, rendering claim 6 obvious. When the switch across the at least one diode connected transistor is closed (or opened depending on where the

switch is located), the corresponding voltage is effectively lowered, causing the switching threshold to be changed. Therefore, the hysteresis circuit effectively lowers the power supply voltage to the comparator of the power up reset circuit, and this changes when the reset signal will be generated, thus claim 7 is also rendered obvious.

Claims 9-12 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Guritz, in view of Furuchi, another reference cited in the previous Office Action. As previously described with respect to claim 4 above, Fig 9 of Guritz shows comparator 14 with its first/second inputs V1/V2 coupled to circuit blocks 18/20, respectively. Since Guritz discloses the various circuit networks shown in Figs. 4a, 4b, 5a, and 5b can be used to provide the desired characteristic curves (e.g. see column 4, lines 35-40), one of ordinary skill in the art would understand that the combination of Figs. 4a/5b, or of Figs. 4b/5a could be used for blocks 18/20. In each combination, power supply VDD will be coupled directly to a first resistor (see the LOAD shown in Figs. 4b and 5b) with the other end of the resistor being connected directly to is corresponding input VR; a first diode connected transistor (see T3 of Fig. 4b, or T2 of Fig. 5b) connected directly to ground, and its other end connected to corresponding input VR; second diode connected transistor (see T1 of Fig. 4a, or T4 of Fig. 5a) coupled directly to power supply VDD, and its other end connected to corresponding input VR; and second resistor (see the LOAD shown in Figs. 4a and 5a) connected directly to ground, with its other end connected to corresponding input VR. However, the reference does not show or disclose reset signal 16 (produced by comparator 14) as being connected to first/second capacitors that are coupled in series between the power supply and ground; or that the IC comprises a Field Programmable Gate Array (FPGA). Column 1, lines 23-38 of Guritz discloses the use of delay circuitry might

possibly be used to minimize premature operation, and column 5, lines 7-12 disclose that various changes and alterations can be made with respect to the spirit and scope of the invention. Furuchi shows and discloses the use of first/second capacitors C1/C2 coupled between power supply Vdd and ground as a delay type means for resisting noise on the power supply or ground (e.g. see the abstract), and with respect to an output of an inverter. In Fig. 3, these two capacitors are coupled to the digital/logical output of inverter 101. Therefore, it would have been obvious to one of ordinary skill in the art to apply the teaching of Furuchi to the circuit of Guritz. In this case, it would have been obvious to couple first capacitor C1 between output node 16 (of Guritz), which corresponds to the output of inverter 30, and power supply VDD, and couple second capacitor C2 between output node 16 and ground, thus rendering independent claim 12 and dependent claim11, obvious. The use of first/second capacitors C1/C2 with Guritz's circuit will help maintain the reset signal at output node 16, even if there is a temporary fluctuation (e.g. noise or a glitch) with respect to either the power supply or ground. The capacitors would also provide a means for adjusting the overall delay of the circuit to ensure the reset signal will not be provided until the power supply voltage has reached its minimum value, after at least a minimum amount of time. One of ordinary skill in the art would understand the output of comparator 14 would be provided at first (or high) and second (or low) logic level output states due to inverter 30, thus rendering claim 10 obvious. Column 5, lines 1-6 of Guritz discloses that the reset signal can be used to clear registers, reset timing, and various other functions "as will be appreciated by those skilled in the art." Therefore, it would have been obvious to one of ordinary skill in the art to use the IC's power up reset circuit with a FPGA, rendering claim 9 obvious. This can be considered intended use, as it is well known to one of ordinary skill in the art that the operation

of a FPGA should not proceed until the power supply has reached at least a minimum, predetermined level. Also, the reset signal can be used to ensure the stored data within a FPGA has been reset, thus avoiding possible indefinite values when the FPGA is used during normal operations after a power up type sequence.

Claims 9-12 remain also rejected under 35 U.S.C. 103(a) as being unpatentable over Frisch et al. (Frisch), in view of Furuchi, for the same reasoning as described above with respect to the rejections of claims 9-12 using the Guritz/Furuchi references. Therefore, it is not considered necessary to basically repeat all the details again other than Furuchi's first/second capacitors C1/C2 could be coupled to output node 41 (or 46) of Frisch to minimize incorrect switching of the reset signal, rendering claims 9-12 obvious.

Allowable Subject Matter

Claims 13, and 19 are allowed, and claim 20 is only objected to as described above. There is no motivation to modify or combine any prior art reference(s) to ensure the circuit includes a hysteresis circuit, with a feedback transistor connected in parallel to a third resistor that is connected to the first diode connected transistor, as recited within claim 13, upon which claims 19-20 depend.

Response to Arguments

The applicant's arguments filed May 10, 2005 have been fully considered but they are not persuasive.

In the present case, the applicant argues that: 1) Frisch does not suggest or teach the use of a plurality of diode-connected transistors, and/or Frisch teaches away from a plurality of diode-connected transistors; 2) there is no motivation to replace a single diode connected

transistor of Guritz with a plurality of diode connected transistors; and 3) nothing in Guritz or Frisch suggests or teaches the use of first/second capacitors connected to the output, and the examiner hasn't pointed out any such language in Guritz or Frisch.

In response to the applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

From the applicant's comments, it appears a single reference must show or suggest everything (or at least a clear objective teaching), even when the claims are rejected under obviousness. Under this type of criteria, if a primary reference discloses or teaches everything, then obviousness rejections would not be necessary because the claims could be rejected under 35 U.S.C. 102. If the reference shows or discloses nothing, then no obvious type rejection can be made. However, the examiner strongly disagrees because when a reference does not clearly show or disclose some type of limitation, that one of ordinary skill in the art would understand and find obvious, the use of obvious type rejections is proper. Therefore, to provide more support to the examiner's reasoning for using a plurality of diode connected transistors, several passages within the main references are included in the rejections described above, along with another reference providing additional support to the knowledge of one of ordinary skill in the art.

The following comments address the various arguments submitted by the applicant:

1) The applicant indicates that Frisch does not teach/suggest a plurality of diode connected transistors, and actually teaches away from them. This appears to be an extremely

narrow interpretation of what is shown and disclosed in Frisch. For example, the abstract does indicate signals tracking a "predetermined threshold", and Fig. 4 does show only a single diode connected transistor in each location, but there is nothing that clearly indicates that the predetermined threshold must be the threshold of only a single diode. A "predetermined threshold" can refer to any predetermined value, which could include the sum of various thresholds related to various combinations (e.g. of transistors, diodes, and/or diode-connected transistors). Also, lines 3-7 of column 9 disclose that those skilled in the art can modify the invention. Since one of ordinary skill in the art knows that a single diode connected transistor can be replaced by two or more diode connected transistors, or vice versa, as one way to change a threshold/voltage drop to obtain a desired level, replacing each single diode connected transistor of Frisch's power-on reset circuit would be obvious. Having one diode connected transistor, or a plurality of diode connected transistors, is not deemed a critical feature of the present invention. The number of diode connected transistors merely provides one means for obtaining the desired operating characteristics with respect to when the comparison of different voltage characteristics will cross, causing the power on reset signal to be generated.

2) Similar to "1)" above, the applicant states that there is no motivation to replace a single diode connected transistor of Guritz with a plurality of diode connected transistors. Guritz cites: 1) each network comprises "at least one field-effect transistor" on lines 32-34 of column 3, thus implying there can be more than one FET in series with the load; 2) "any combination of elements" can be used to provide the reference voltage curves that cross within the desired range on lines 30-32 of column 4; and 3) changes and alterations can be made "without departing from the spirit and scope of the invention" on lines 8-11 of column 5. Therefore, it is not understood

by this examiner why it would not be obvious to one of ordinary skill in the art to replace a single diode-connected transistor with a plurality of diode connected transistors within Guritz's circuit.

3) The use of capacitors at an output of a circuit is one well known means for helping to minimize fluctuations at the output that can be caused by power supply, or ground, related noise or variations. Just because the references of Guritz or Frisch do not clearly suggest or teach the use of capacitors at the output, this does not preclude one of ordinary skill in the art from using known means. The Furuchi reference is cited as one example showing/disclosing first/second capacitors coupled to an output of a circuit (e.g. inverter). Again, from this examiner's perspective, the applicant appears to be implying a reference must clearly show, disclose, or suggest every claimed variation, even if that limitation is not a critical type feature of the claimed invention, and is a known feature one of ordinary skill in the art would find obvious to use under various circumstances (e.g. desire to change threshold voltages; minimizing inadvertent triggering; etc.).

Therefore, the rejections described in this Office Action are deemed proper with respect to the broadest reasonable interpretation of the claimed limitations, and the knowledge of one of ordinary skill in the art.

THIS ACTION IS MADE FINAL. The applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund
22 July 2005

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800